

IN THE CLAIMS:

Applicant notes that the listing of claims indicates that claims 13-20 stand withdrawn per the Examiner's indication, yet maintains the traversals of the restriction requirement, which was improper as further detailed in the Remarks that follow.

CLAIMS

1. (Currently Amended) A method of fabricating an integrated circuit, the method comprising:
 - providing a substrate;
 - creating at least one base-window in a layer to expose a surface of the substrate;
 - forming a monocrystalline SiGe layer in at least one region of the base-window on the exposed surface of the substrate;[[,]] and
 - forming a polycrystalline SiGe layer elsewhere over the substrate.
2. (Previously presented) A method as recited in claim 1, further comprising forming a polycrystalline silicon layer over selectively exposed portions of the substrate.
3. (Previously presented) A method as recited in claim 2, further comprising forming a mask over a top surface, providing openings in selected locations of the mask, and removing the polycrystalline silicon layer to expose the selected portions of the substrate.
4. (Previously presented) A method as recited in claim 3, wherein the exposed portions of the substrate are monocrystalline silicon.
5. (Previously presented) A method as recited in claim 1, wherein the integrated circuit includes a lateral pnp transistor.
6. (Previously presented) A method as recited in claim 1, wherein the integrated circuit includes an SiGe bipolar transistor.
7. (Previously presented) A method as recited in claim 6, wherein the SiGe bipolar

transistor includes the monocrystalline SiGe.

8. (Previously presented) A method as recited in claim 1, wherein the integrated circuit includes a varactor diode.

9. (Previously presented) A method as recited in claim 1, further comprising forming a polysilicon resistor.

10. (Previously presented) A method as recited in claim 1, wherein only one masking step is required to form a lateral pnp transistor, varactor diode and a polysilicon resistor.

11. (Previously presented) A method as recited in claim 10, wherein the lateral pnp transistor is a silicon device, and includes a portion of the polycrystalline SiGe layer in each of a collector contact and an emitter contact.

12. (Previously presented) A method as recited in claim 11, wherein the polycrystalline SiGe layer is disposed beneath a polycrystalline silicon layer.

13. (Withdrawn) A method of fabricating a semiconductor structure, the method comprising:

- forming a silicon seed layer over a surface of a substrate;
- providing openings in the seed layer;
- selectively forming amorphous silicon over the substrate; and
- forming monocrystalline SiGe.

14. (Withdrawn) A method as recited in claim 13, further comprising, removing said amorphous silicon in regions where said monocrystalline SiGe is formed.

15. (Withdrawn) A method as recited in claim 14, wherein said removing said amorphous silicon exposes a top surface of the substrate.

16. (Withdrawn) A method as recited in claim 15, wherein the top surface is

monocrystalline silicon.

17. (Withdrawn) A method as recited in claim 13, wherein the semiconductor structure includes a lateral pnp transistor.

18. (Withdrawn) A method as recited in claim 13, wherein the semiconductor structure includes a SiGe bipolar transistor.

19. (Withdrawn) A method as recited in claim 13, wherein the semiconductor structure includes a varactor diode.

20. (Withdrawn) A method as recited in claim 13, further comprising forming a polysilicon resistor.